FIG.1A

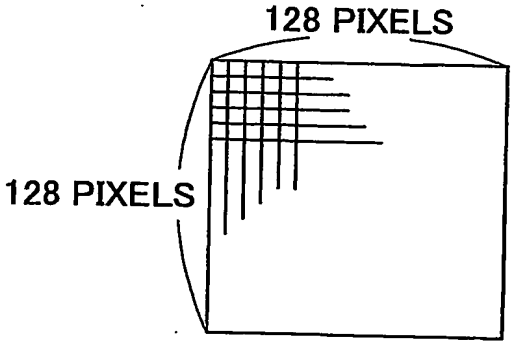


FIG.1B

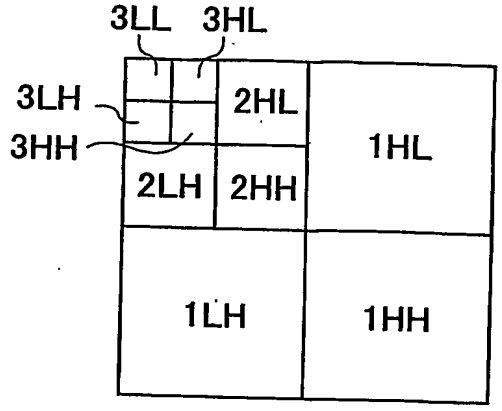


FIG.1C

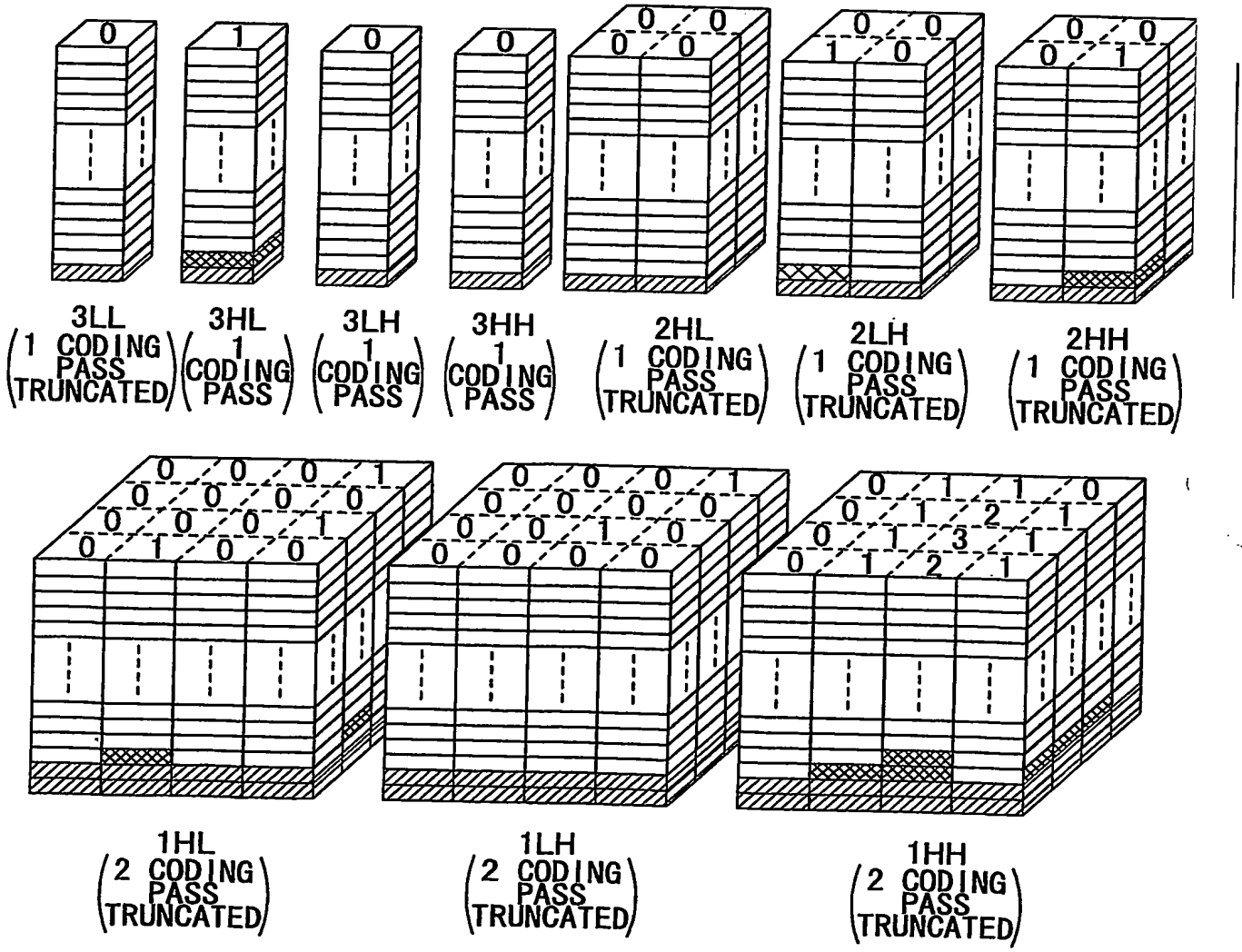


FIG.2

T	Y 3LL, 3HL-LH-HH, 2HL-LH-HH, 1HL-LH-HH Cb 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH Cr 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH	T	Y 3LL, 3HL-LH-HH, 2HL-LH-HH, 1HL-LH-HH Cb 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH Cr 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH
T=0	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 1 0, 0 0 0, 0 0 0, 0 0 0	T=399	1, 1 1 3, 4 4 6, 101017 9, 101013, 141418, 202027 8, 9 911, 121216, 181823
T=1	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 2 0, 0 0 0, 0 0 0, 0 0 0	T=400	1, 1 1 3, 4 4 6, 101017 9, 101013, 141418, 202027 8, 9 911, 121216, 181823
T=2	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 3 0, 0 0 0, 0 0 0, 0 0 0	⋮	⋮
⋮	⋮	T=499	
T=99	0, 0 0 0, 0 0 0, 0 0 6 0, 0 0 3, 4 4 8, 101017 0, 0 0 1, 2 2 6, 7 713	T=500	
T=100	0, 0 0 0, 0 0 0, 0 0 7 0, 0 0 3, 4 4 8, 101017 0, 0 0 1, 2 2 6, 7 713	⋮	⋮
⋮	⋮	T=1000	
T=199	0, 0 0 0, 0 0 0, 5 511 3, 4 4 7, 8 813, 151521 2, 3 3 6, 7 710, 121217	⋮	⋮
T=200	0, 0 0 0, 0 0 0, 5 511 3, 4 4 7, 8 813, 151522 2, 3 3 6, 7 710, 121217	T=1500	
⋮	⋮	⋮	⋮
T=299	0, 0 0 0, 1 1 4, 8 814 6, 7 710, 111216, 181825 6, 6 6 9, 101013, 151520	⋮	⋮
T=300	0, 0 0 0, 1 1 4, 8 814 6, 7 710, 121216, 181825 6, 6 6 9, 101013, 151520	⋮	⋮
⋮	⋮	⋮	⋮

FIG.3

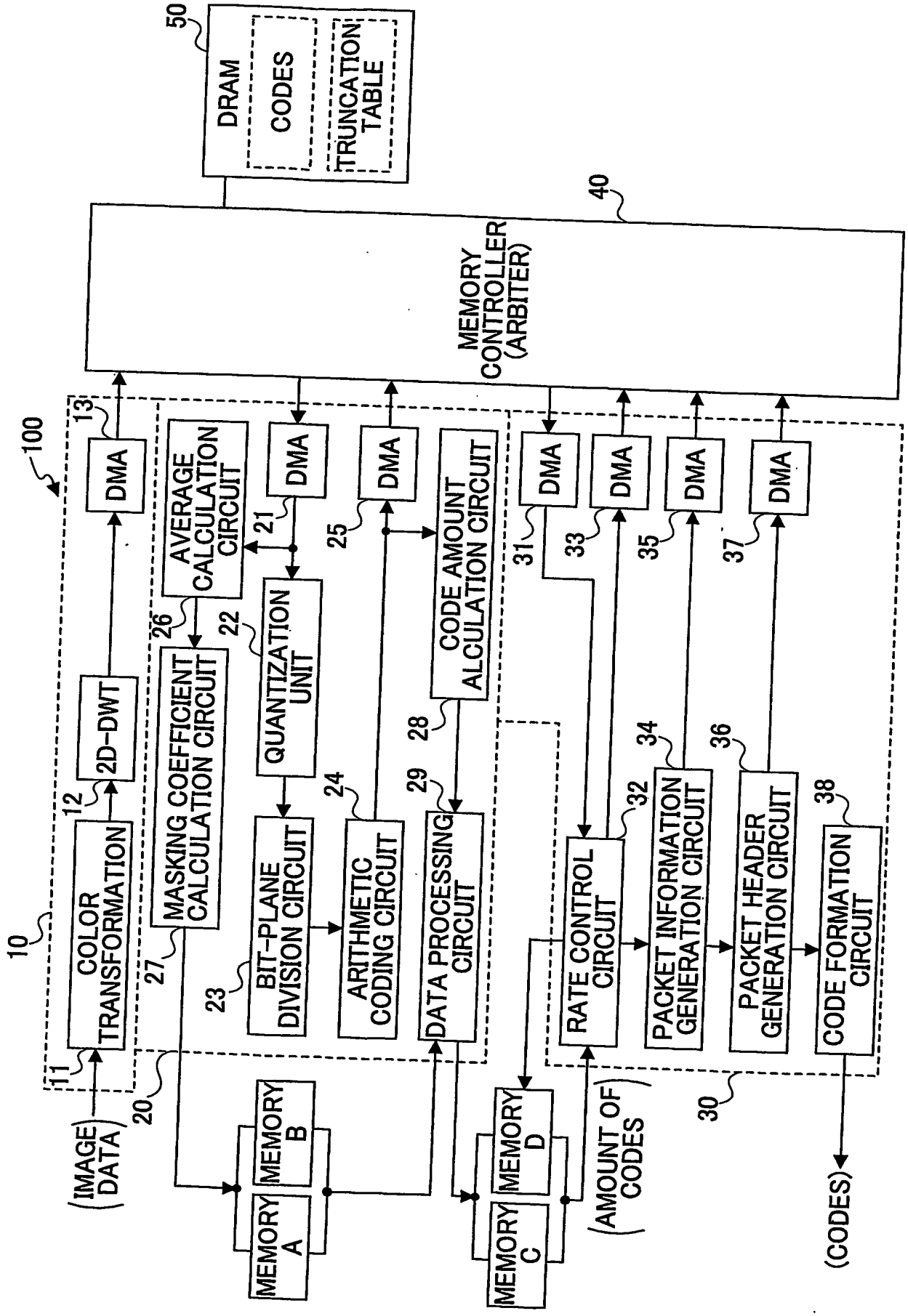

50
DRAM
CODES
TRUNCATION TABLE
40
MEMORY CONTROLLER (ARBITER)
100
10
13
DMA
12
2D-DWT
11
COLOR TRANSFORMATION
20
(IMAGE DATA)
AVERAGE CALCULATION CIRCUIT
21
26
MASKING COEFFICIENT CALCULATION CIRCUIT
27
22
QUANTIZATION UNIT
23
BIT-PLANE DIVISION CIRCUIT
24
ARITHMETIC CODING CIRCUIT
25
CODE AMOUNT ALCULATION CIRCUIT
28
29
DATA PROCESSING CIRCUIT
31
33
35
37
RATE CONTROL CIRCUIT
32
PACKET INFORMATION GENERATION CIRCUIT
34
PACKET HEADER GENERATION CIRCUIT
36
CODE FORMATION CIRCUIT
38
30
(CODES)
(AMOUNT OF CODES)
MEMORY A
MEMORY B
MEMORY C
MEMORY D

FIG.4

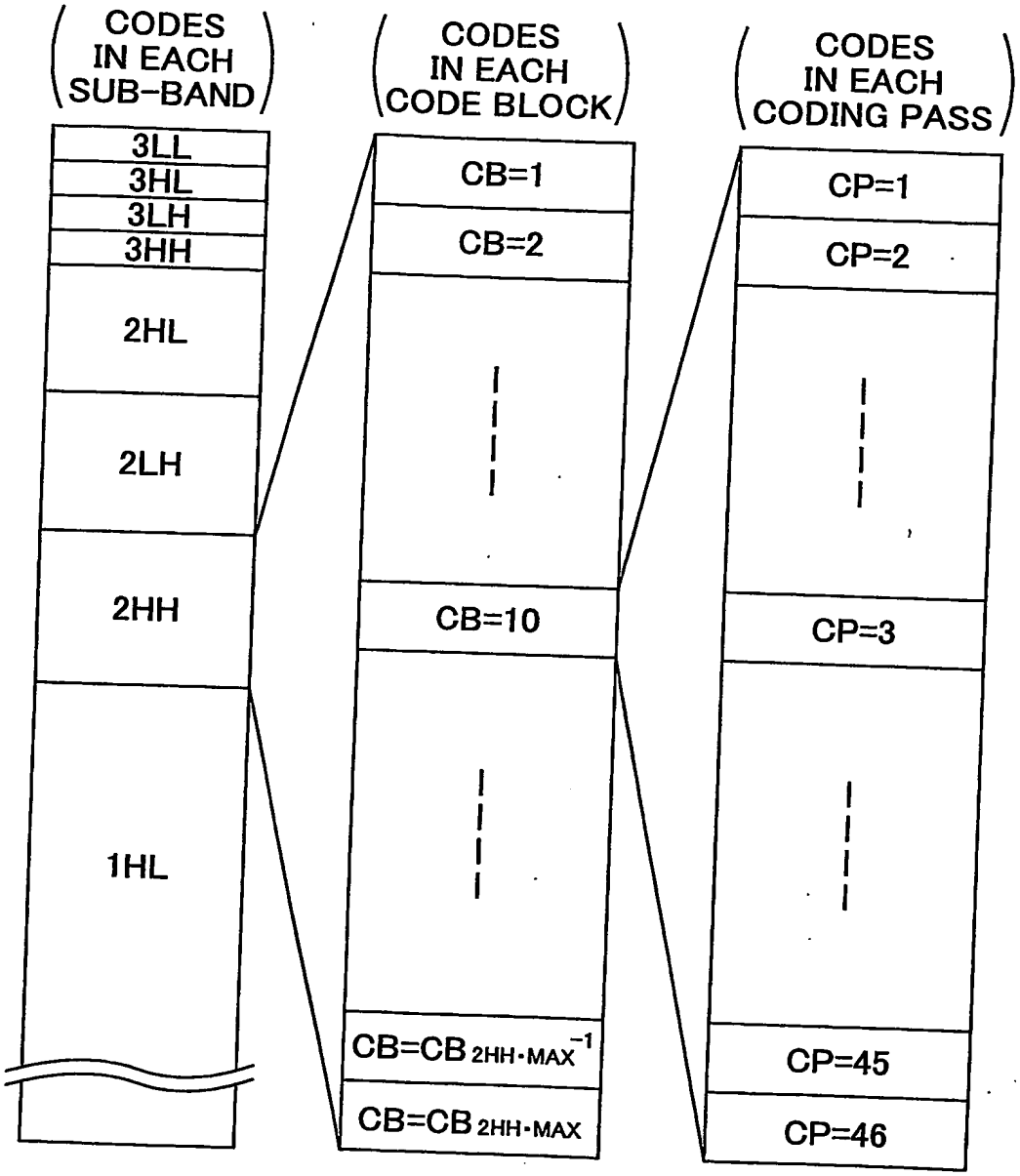

CODES IN EACH SUB-BAND
3LL
3HL
3LH
3HH
2HL
2LH
2HH
1HL
CODES IN EACH CODE BLOCK
CB=1
CB=2
CB=10
CB=CB 2HH·MAX -1
CB=CB 2HH·MAX
CODES IN EACH CODING PASS
CP=1
CP=2
CP=3
CP=45
CP=46

FIG.5

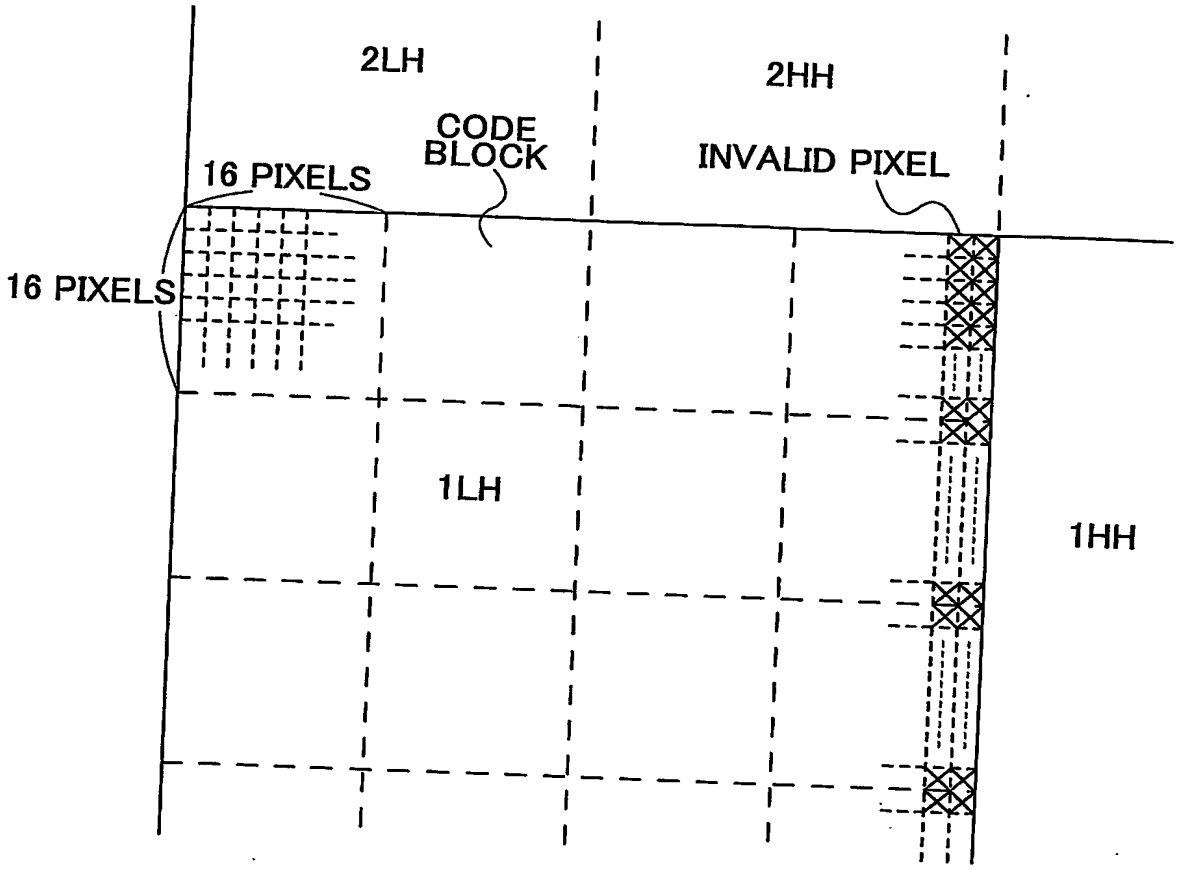


FIG.6

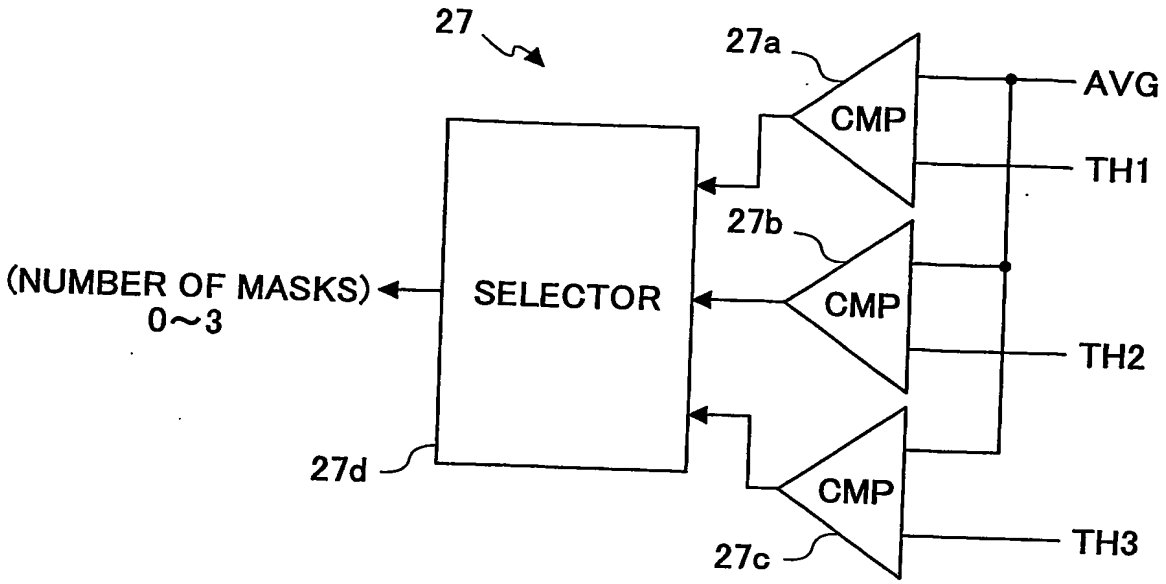

27
27a
CMP
AVG
TH1
27b
CMP
TH2
(NUMBER OF MASKS)
0～3
SELECTOR
27d
CMP
TH3
27c

FIG.7

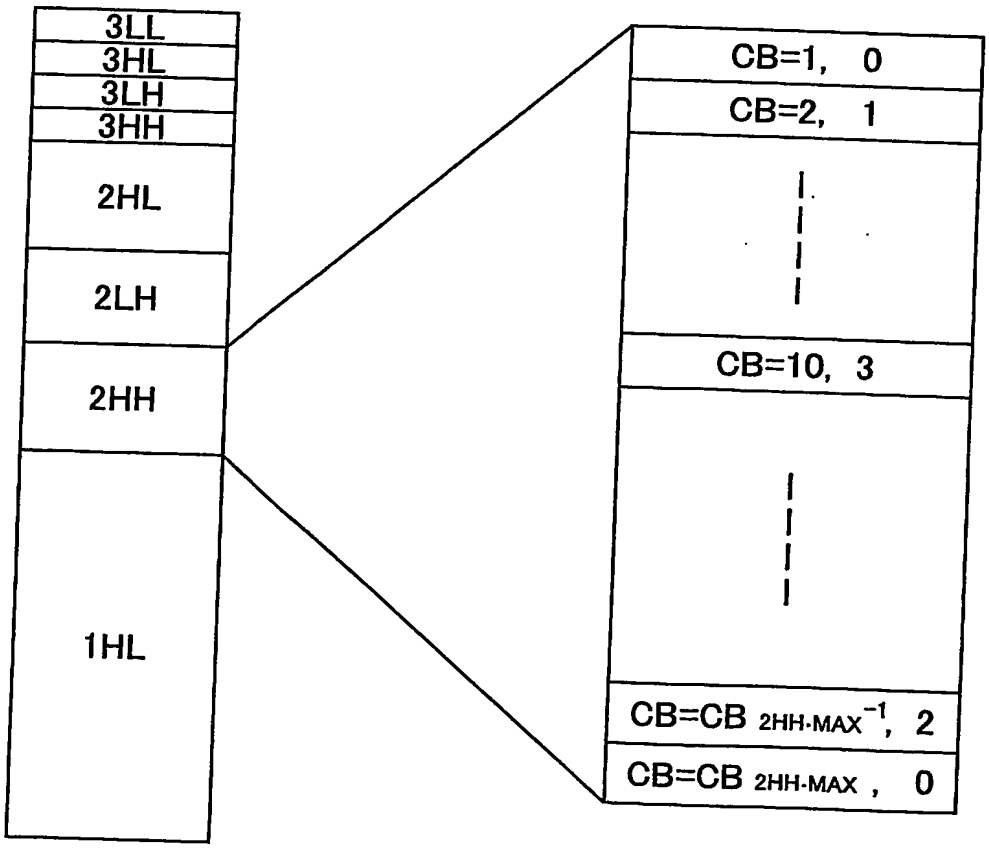

3LL
3HL
3LH
3HH
2HL
2LH
2HH
1HL
CB=1, 0
CB=2, 1
CB=10, 3
CB=CB 2HH-MAX-1, 2
CB=CB 2HH-MAX , 0

FIG.8

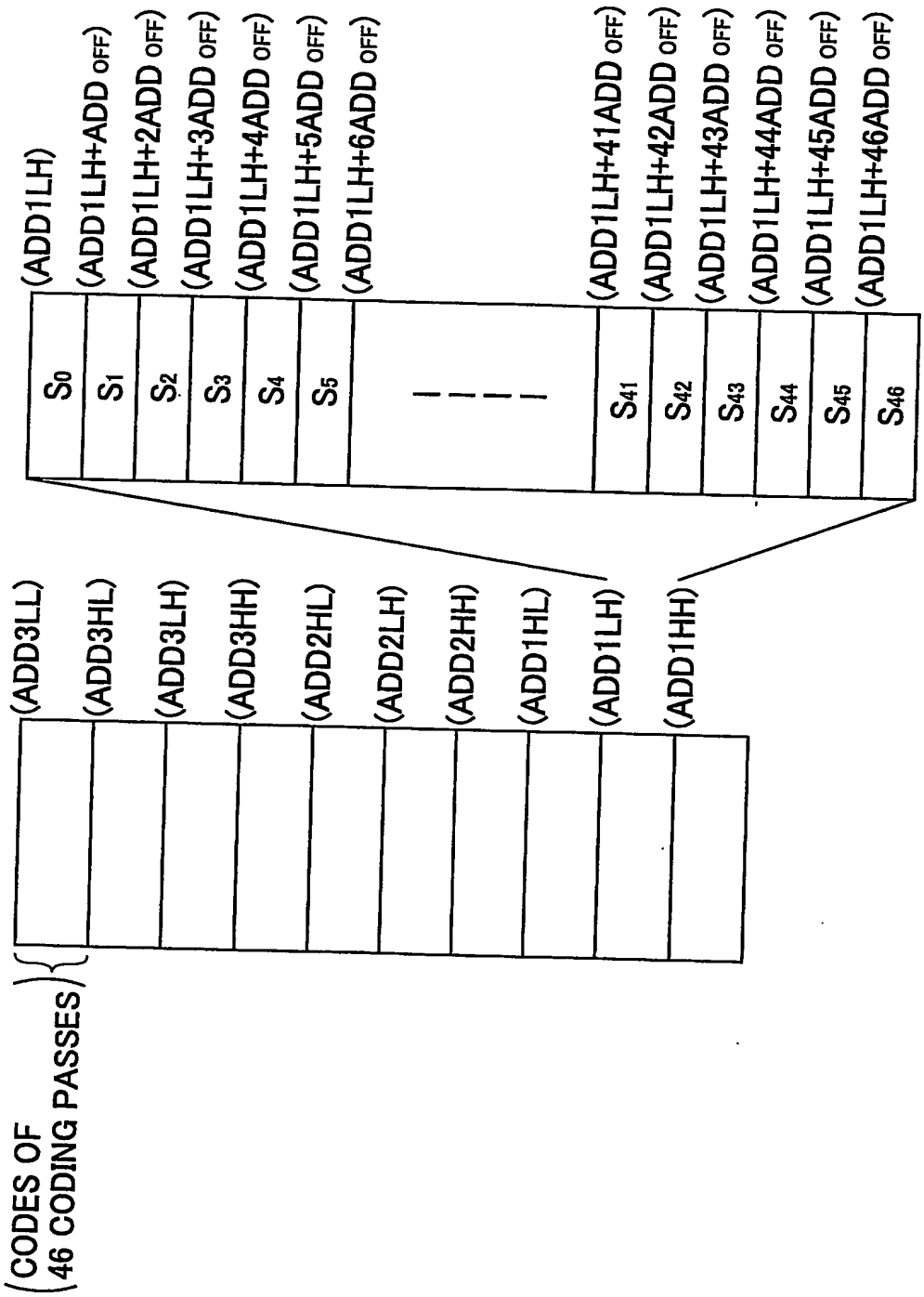

(CODES OF 46 CODING PASSES)
(ADD3LL)
(ADD3HL)
(ADD3LH)
(ADD3HH)
(ADD2HL)
(ADD2LH)
(ADD2HH)
(ADD1HL)
(ADD1LH)
(ADD1HH)
(ADD1LH)
(ADD1LH+ADD OFF)
(ADD1LH+2ADD OFF)
(ADD1LH+3ADD OFF)
(ADD1LH+4ADD OFF)
(ADD1LH+5ADD OFF)
(ADD1LH+6ADD OFF)
(ADD1LH+41ADD OFF)
(ADD1LH+42ADD OFF)
(ADD1LH+43ADD OFF)
(ADD1LH+44ADD OFF)
(ADD1LH+45ADD OFF)
(ADD1LH+46ADD OFF)
S0
S1
S2
S3
S4
S5
S41
S42
S43
S44
S45
S46

FIG.9

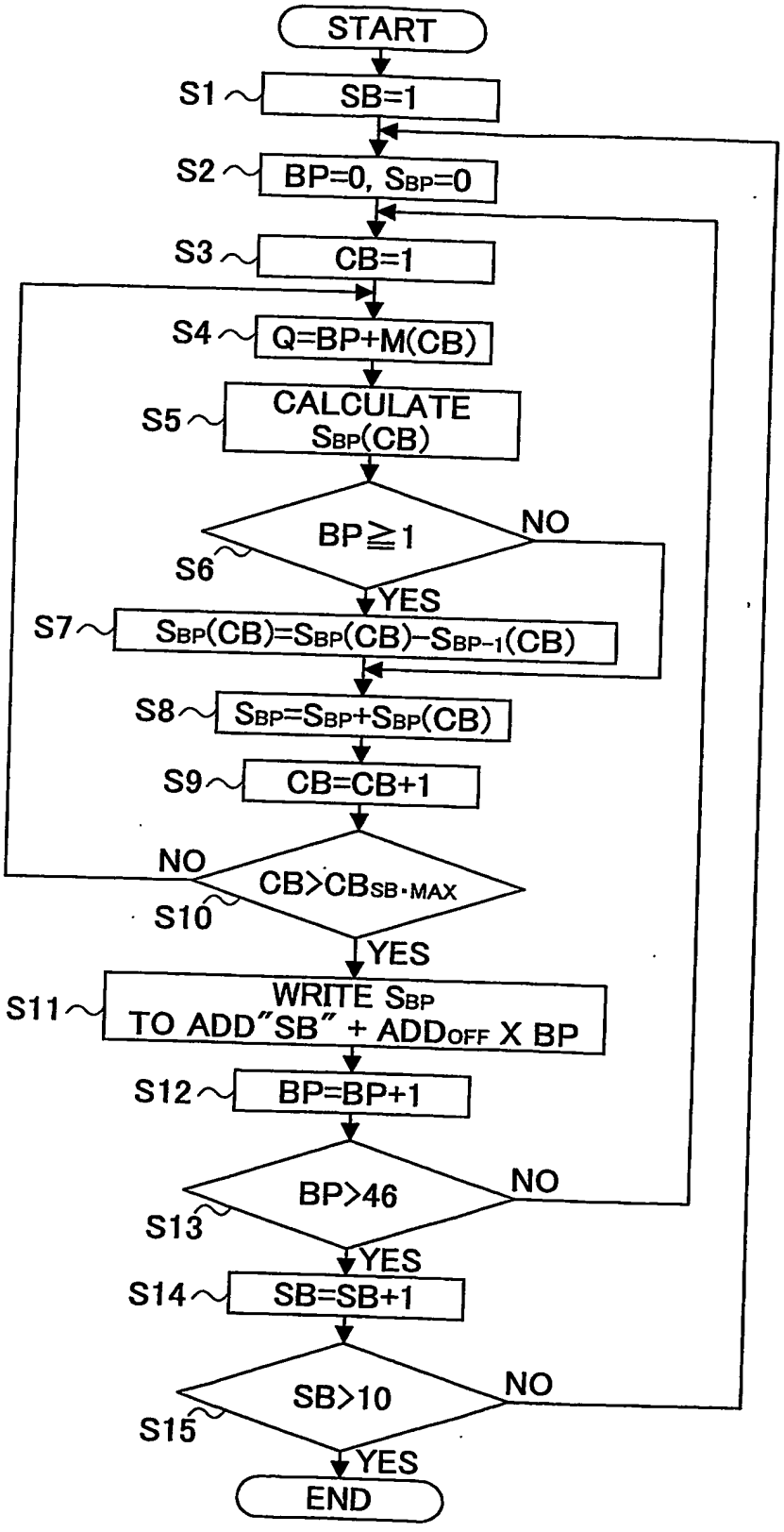

START
S1
SB=1
S2
BP=0, SBP=0
S3
CB=1
S4
Q=BP+M(CB)
S5
CALCULATE SBP(CB)
S6
BP≧1
NO
YES
S7
SBP(CB)=SBP(CB)-SBP-1(CB)
S8
SBP=SBP+SBP(CB)
S9
CB=CB+1
S10
CB>CBSB·MAX
NO
YES
S11
WRITE SBP TO ADD"SB" + ADDOFF X BP
S12
BP=BP+1
S13
BP>46
NO
YES
S14
SB=SB+1
S15
SB>10
NO
YES
END

FIG.10

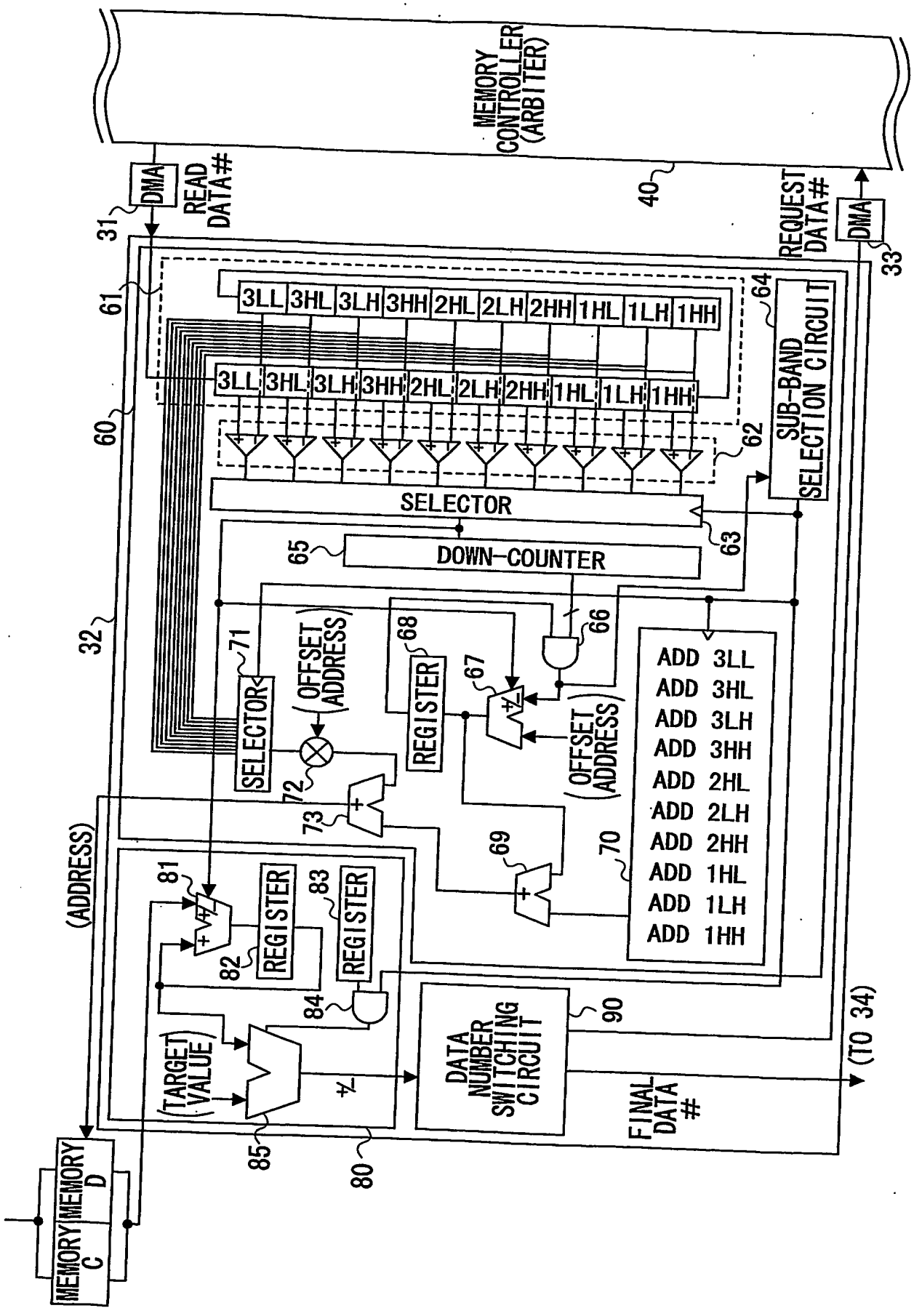

MEMORY CONTROLLER (ARBITER)
40
DMA
READ DATA#
31
REQUEST DATA#
DMA
33
61
3LL 3HL 3LH 3HH 2HL 2LH 2HH 1HL 1LH 1HH
64
SUB-BAND SELECTION CIRCUIT
60
62
SELECTOR
63
65
DOWN-COUNTER
32
71
SELECTOR
OFFSET ADDRESS
68
REGISTER
67
66
OFFSET ADDRESS
ADD 3LL
ADD 3HL
ADD 3LH
ADD 3HH
ADD 2HL
ADD 2LH
ADD 2HH
ADD 1HL
ADD 1LH
ADD 1HH
72
73
69
70
(ADDRESS)
81
82
REGISTER
83
REGISTER
84
(TARGET VALUE)
85
80
DATA NUMBER SWITCHING CIRCUIT
90
FINAL DATA #
(TO 34)
MEMORY D
MEMORY C

FIG.11

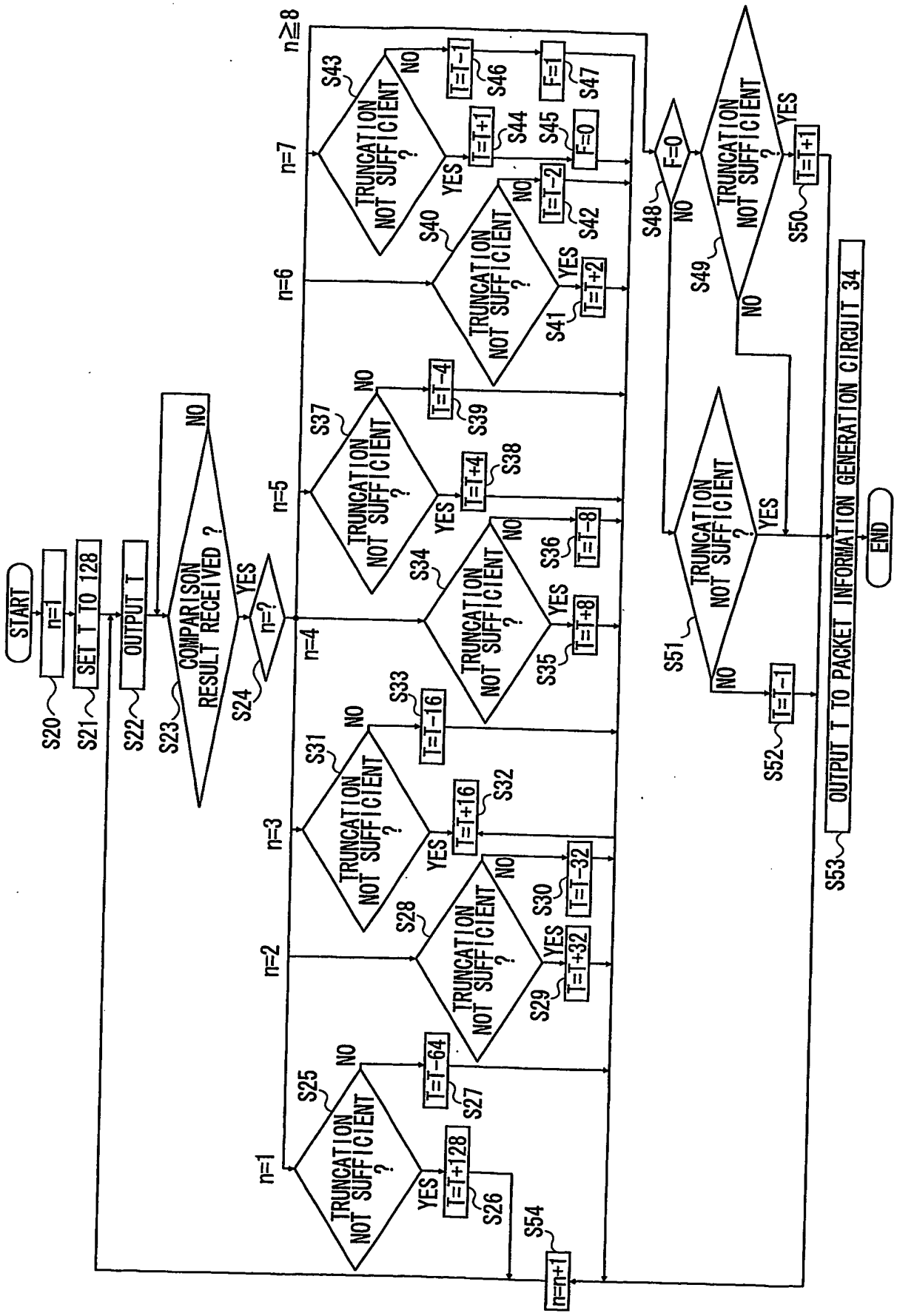

START
n=1
SET T TO 128
OUTPUT T
COMPARISON RESULT RECEIVED ?
NO
YES
n=?
n≧8
n=7
n=6
n=5
n=4
n=3
n=2
n=1
TRUNCATION NOT SUFFICIENT ?
T=T+128
T=T-64
T=T+32
T=T-32
T=T+16
T=T-16
T=T+8
T=T-8
T=T+4
T=T-4
T=T+2
T=T-2
T=T+1
T=T-1
F=1
F=0
n=n+1
OUTPUT T TO PACKET INFORMATION GENERATION CIRCUIT 34
END
S20
S21
S22
S23
S24
S25
S26
S27
S28
S29
S30
S31
S32
S33
S34
S35
S36
S37
S38
S39
S40
S41
S42
S43
S44
S45
S46
S47
S48
S49
S50
S51
S52
S53
S54

FIG.12

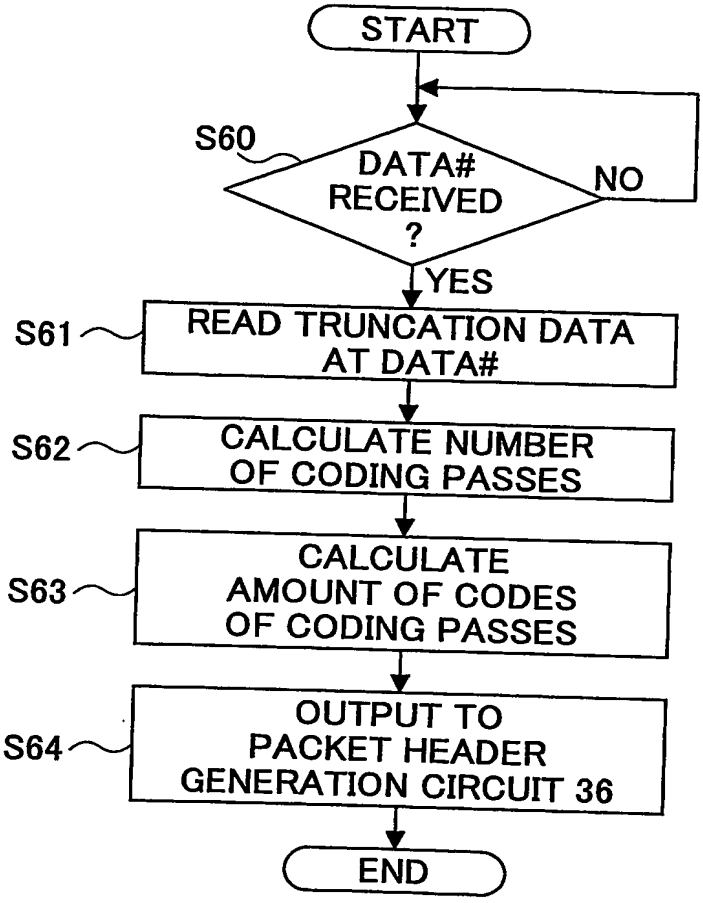

START
S60
DATA# RECEIVED ?
NO
YES
S61
READ TRUNCATION DATA AT DATA#
S62
CALCULATE NUMBER OF CODING PASSES
S63
CALCULATE AMOUNT OF CODES OF CODING PASSES
S64
OUTPUT TO PACKET HEADER GENERATION CIRCUIT 36
END

FIG.13

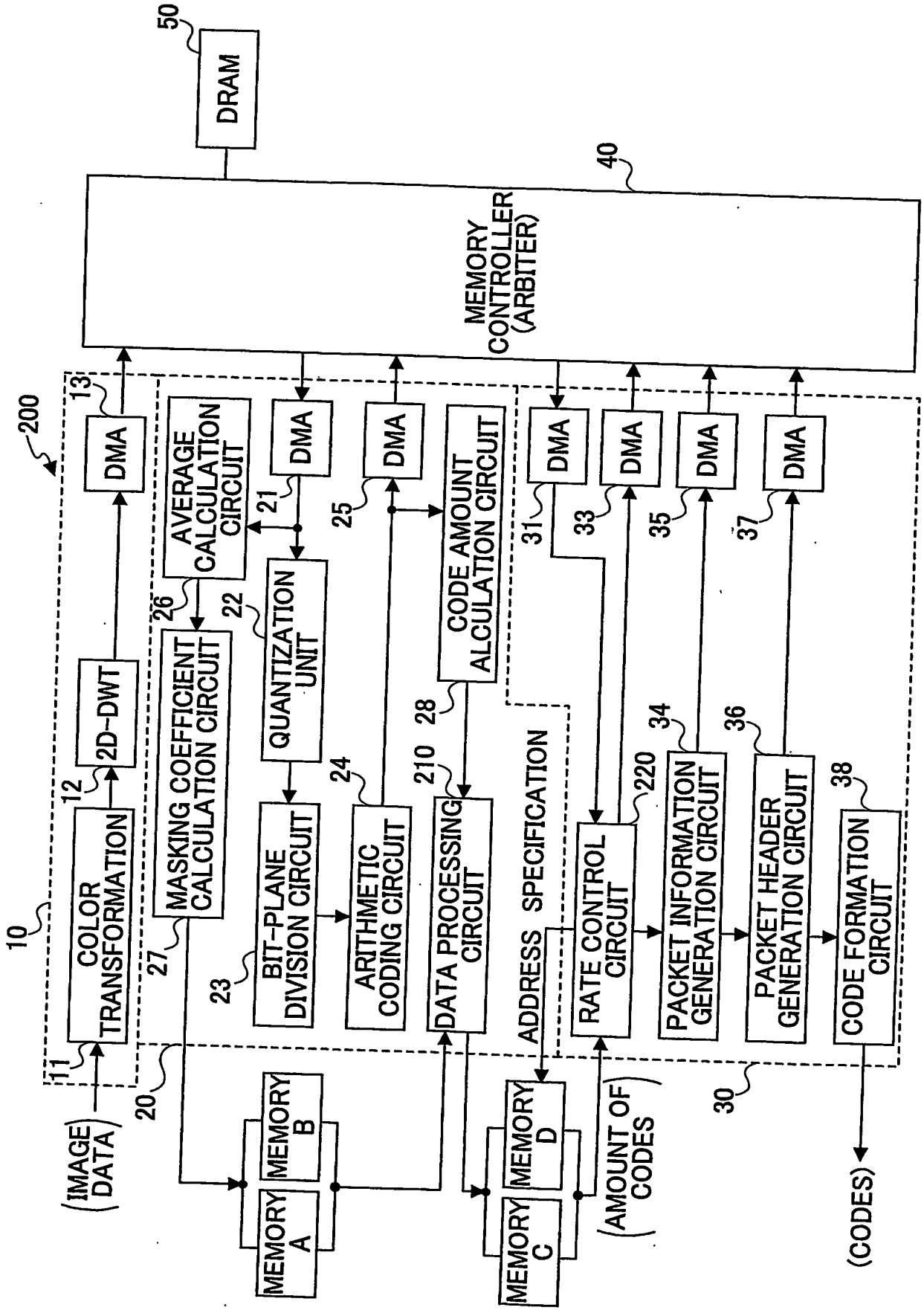

50
DRAM
40
MEMORY CONTROLLER (ARBITER)
200
10
13
DMA
12
2D-DWT
11
COLOR TRANSFORMATION
20
(IMAGE DATA)
AVERAGE CALCULATION CIRCUIT
21
26
MASKING COEFFICIENT CALCULATION CIRCUIT
27
22
QUANTIZATION UNIT
23
BIT-PLANE DIVISION CIRCUIT
24
ARITHMETIC CODING CIRCUIT
25
CODE AMOUNT ALCULATION CIRCUIT
28
210
DATA PROCESSING CIRCUIT
ADDRESS SPECIFICATION
31
33
35
37
220
RATE CONTROL CIRCUIT
34
PACKET INFORMATION GENERATION CIRCUIT
36
PACKET HEADER GENERATION CIRCUIT
38
CODE FORMATION CIRCUIT
30
(CODES)
(AMOUNT OF CODES)
MEMORY A
MEMORY B
MEMORY C
MEMORY D

FIG.14

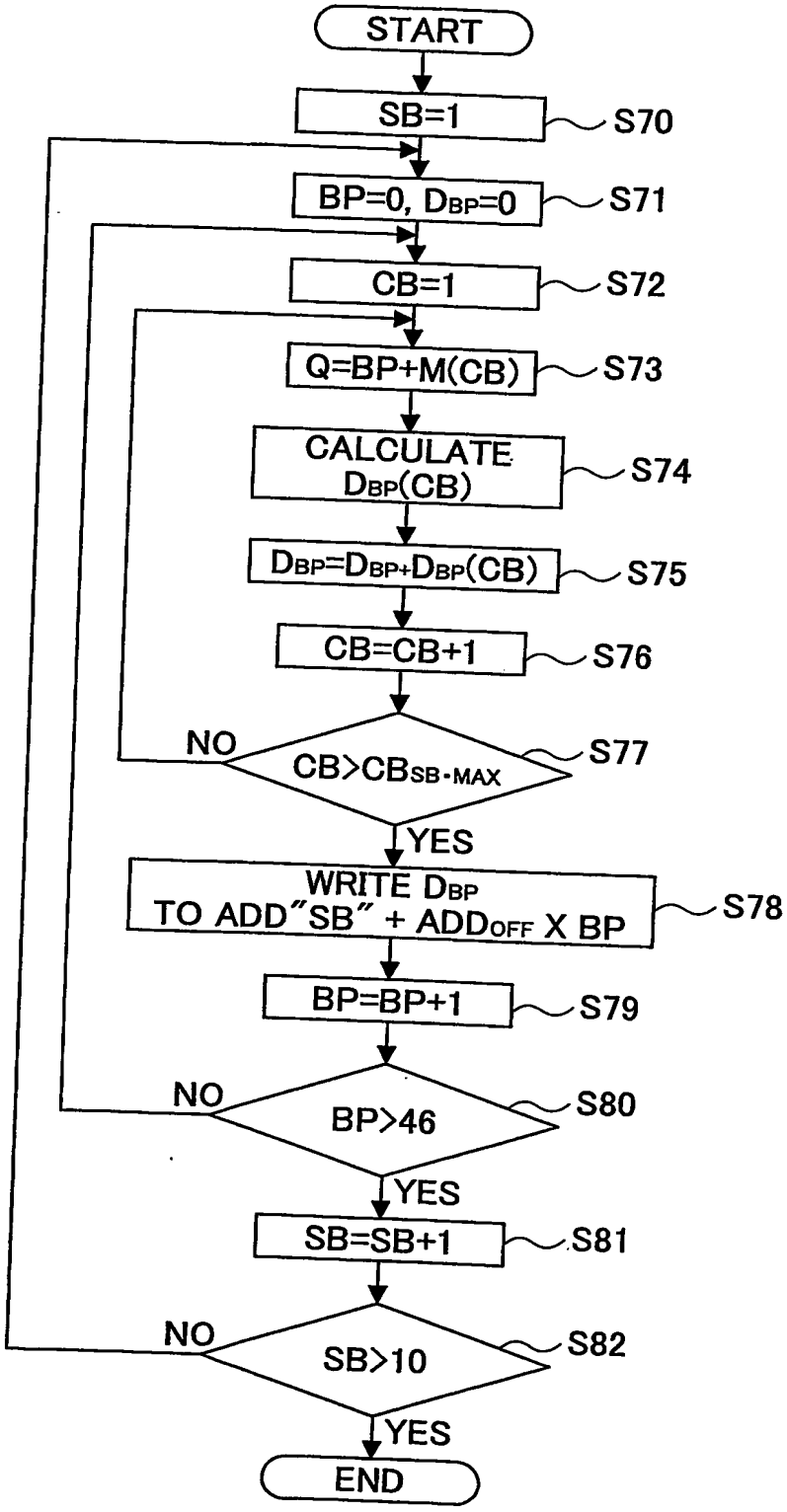

START
SB=1
S70
BP=0, DBP=0
S71
CB=1
S72
Q=BP+M(CB)
S73
CALCULATE DBP(CB)
S74
DBP=DBP+DBP(CB)
S75
CB=CB+1
S76
NO
CB>CBSB·MAX
S77
YES
WRITE DBP TO ADD"SB" + ADDOFF X BP
S78
BP=BP+1
S79
NO
BP>46
S80
YES
SB=SB+1
S81
NO
SB>10
S82
YES
END

FIG.15

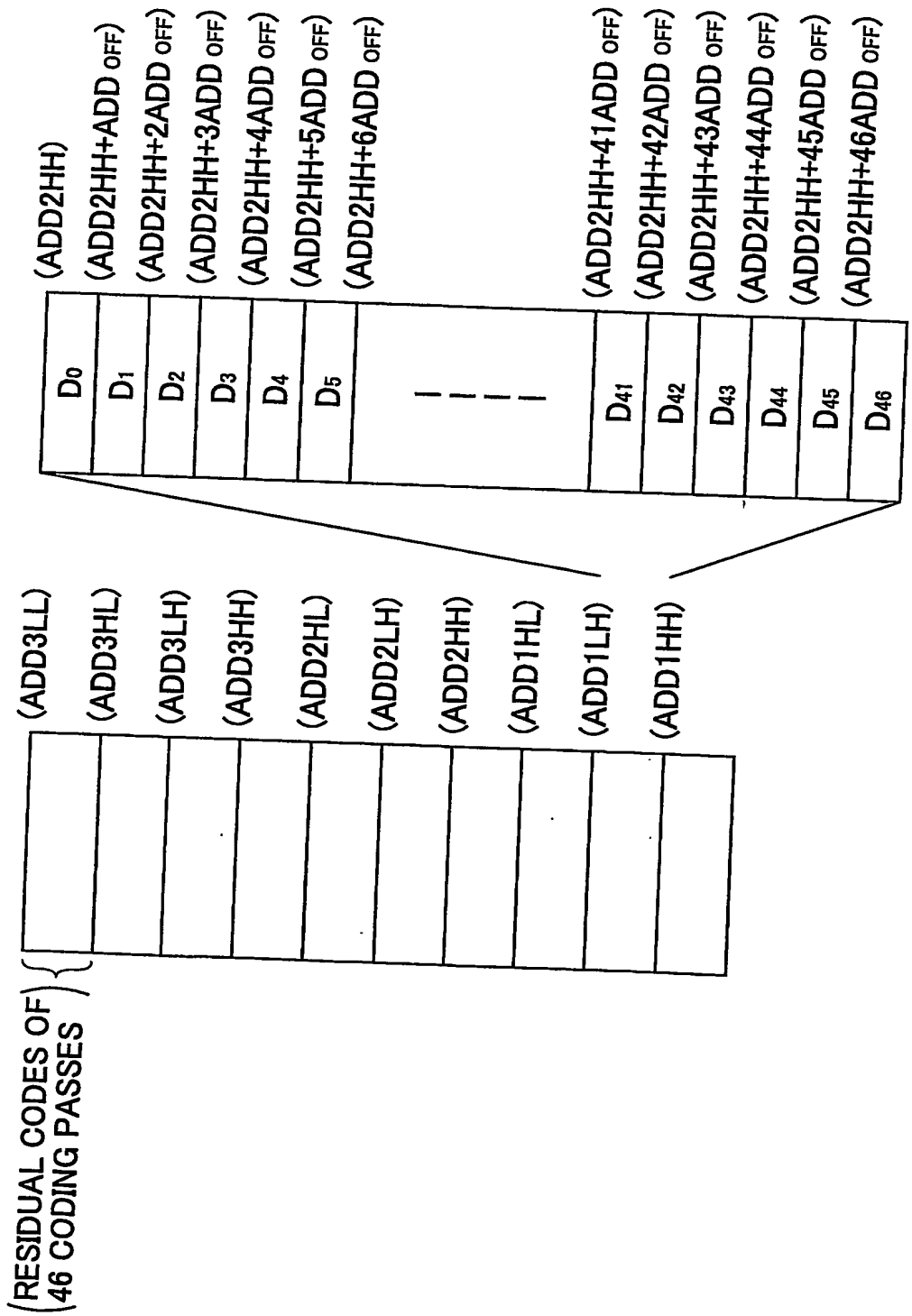

(RESIDUAL CODES OF 46 CODING PASSES)
(ADD3LL)
(ADD3HL)
(ADD3LH)
(ADD3HH)
(ADD2HL)
(ADD2LH)
(ADD2HH)
(ADD1HL)
(ADD1LH)
(ADD1HH)
D0
D1
D2
D3
D4
D5
D41
D42
D43
D44
D45
D46
(ADD2HH)
(ADD2HH+ADD OFF)
(ADD2HH+2ADD OFF)
(ADD2HH+3ADD OFF)
(ADD2HH+4ADD OFF)
(ADD2HH+5ADD OFF)
(ADD2HH+6ADD OFF)
(ADD2HH+41ADD OFF)
(ADD2HH+42ADD OFF)
(ADD2HH+43ADD OFF)
(ADD2HH+44ADD OFF)
(ADD2HH+45ADD OFF)
(ADD2HH+46ADD OFF)

FIG.16

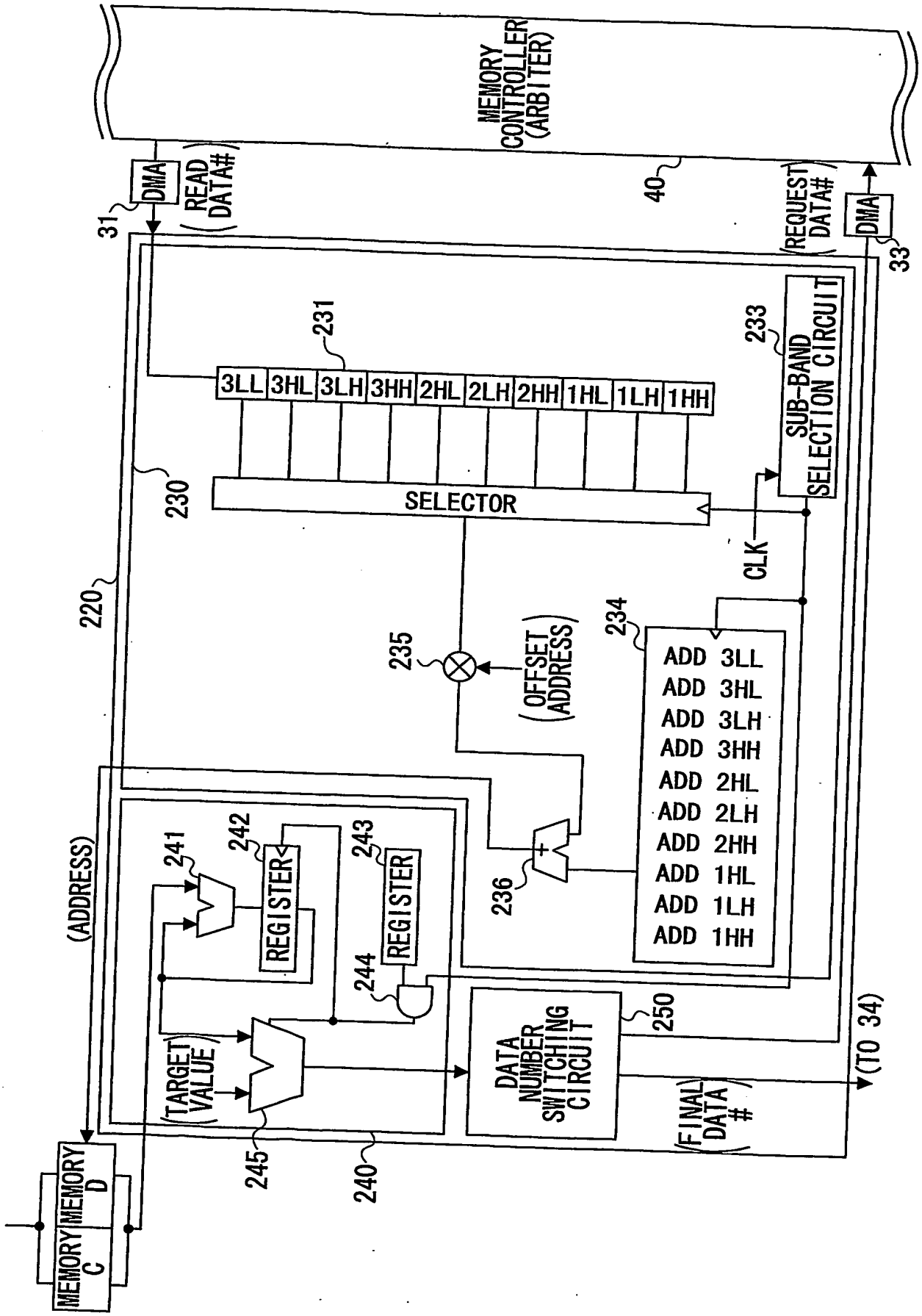

MEMORY CONTROLLER (ARBITER)
40
DMA
31
READ DATA#
REQUEST DATA#
DMA
33
231
233
SUB-BAND SELECTION CIRCUIT
3LL 3HL 3LH 3HH 2HL 2LH 2HH 1HL 1LH 1HH
230
SELECTOR
CLK
220
235
OFFSET ADDRESS
234
ADD 3LL
ADD 3HL
ADD 3LH
ADD 3HH
ADD 2HL
ADD 2LH
ADD 2HH
ADD 1HL
ADD 1LH
ADD 1HH
236
(ADDRESS)
241
242
REGISTER
243
REGISTER
244
TARGET VALUE
245
240
DATA NUMBER SWITCHING CIRCUIT
250
(TO 34)
FINAL DATA #
MEMORY C
MEMORY D

FIG.17

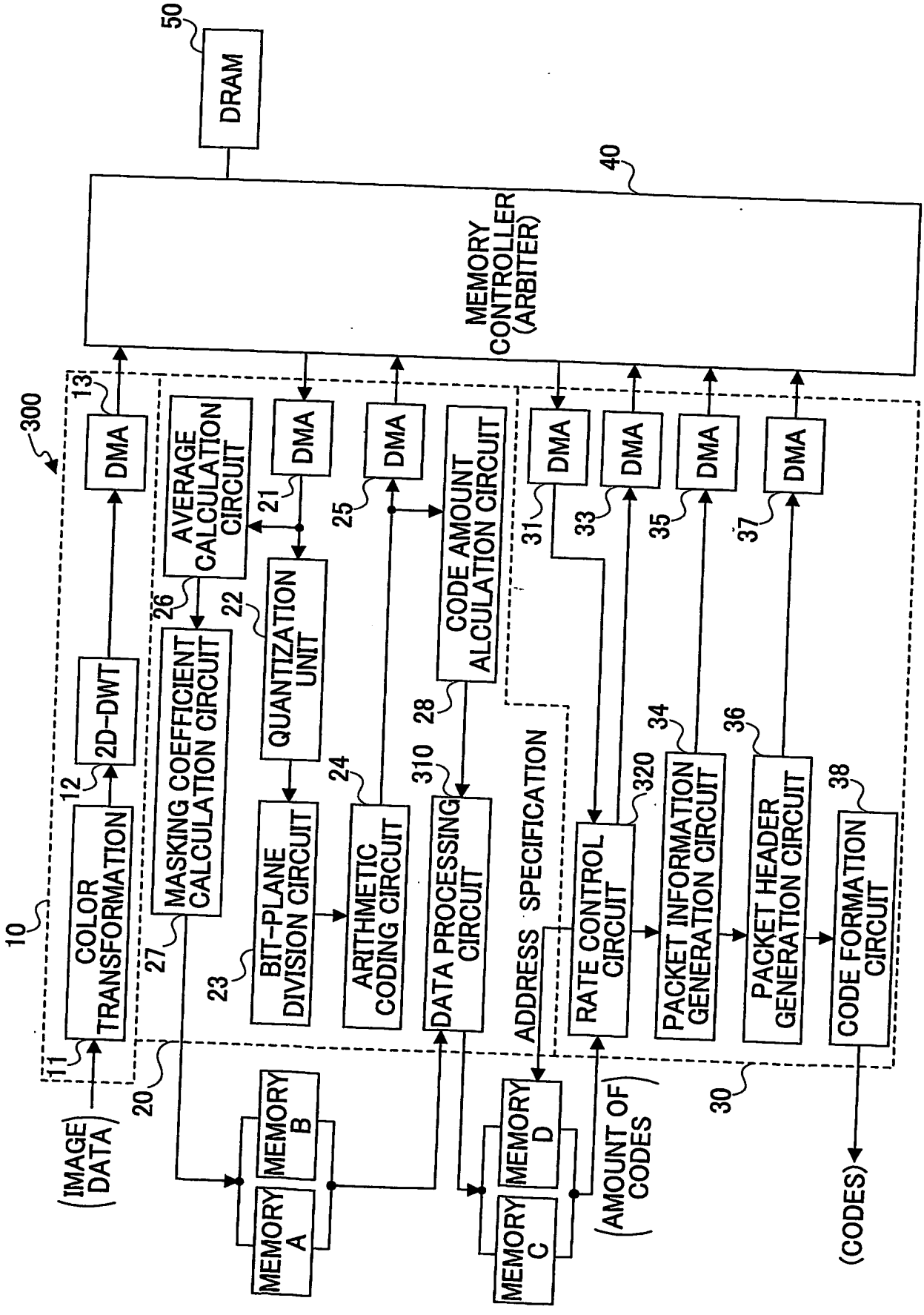

50
DRAM
40
MEMORY CONTROLLER (ARBITER)
300
10
13
DMA
12
2D-DWT
11
COLOR TRANSFORMATION
(IMAGE DATA)
20
AVERAGE CALCULATION CIRCUIT
21
DMA
26
MASKING COEFFICIENT CALCULATION CIRCUIT
27
22
QUANTIZATION UNIT
23
BIT-PLANE DIVISION CIRCUIT
24
ARITHMETIC CODING CIRCUIT
25
DMA
28
CODE AMOUNT ALCULATION CIRCUIT
310
DATA PROCESSING CIRCUIT
ADDRESS SPECIFICATION
MEMORY A
MEMORY B
MEMORY C
MEMORY D
31
DMA
33
DMA
320
RATE CONTROL CIRCUIT
(AMOUNT OF CODES)
34
PACKET INFORMATION GENERATION CIRCUIT
35
DMA
36
PACKET HEADER GENERATION CIRCUIT
37
DMA
38
CODE FORMATION CIRCUIT
30
(CODES)

FIG.18

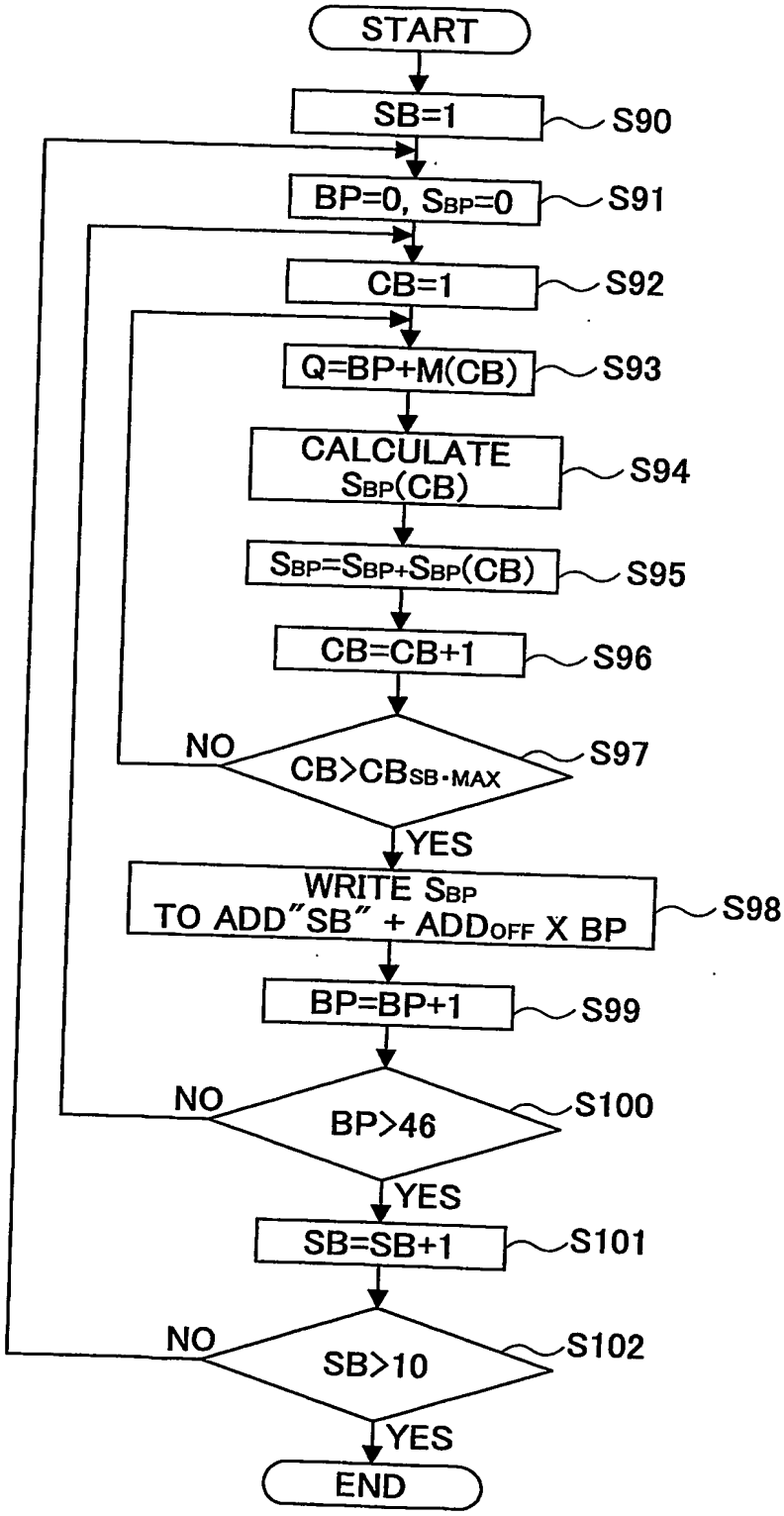
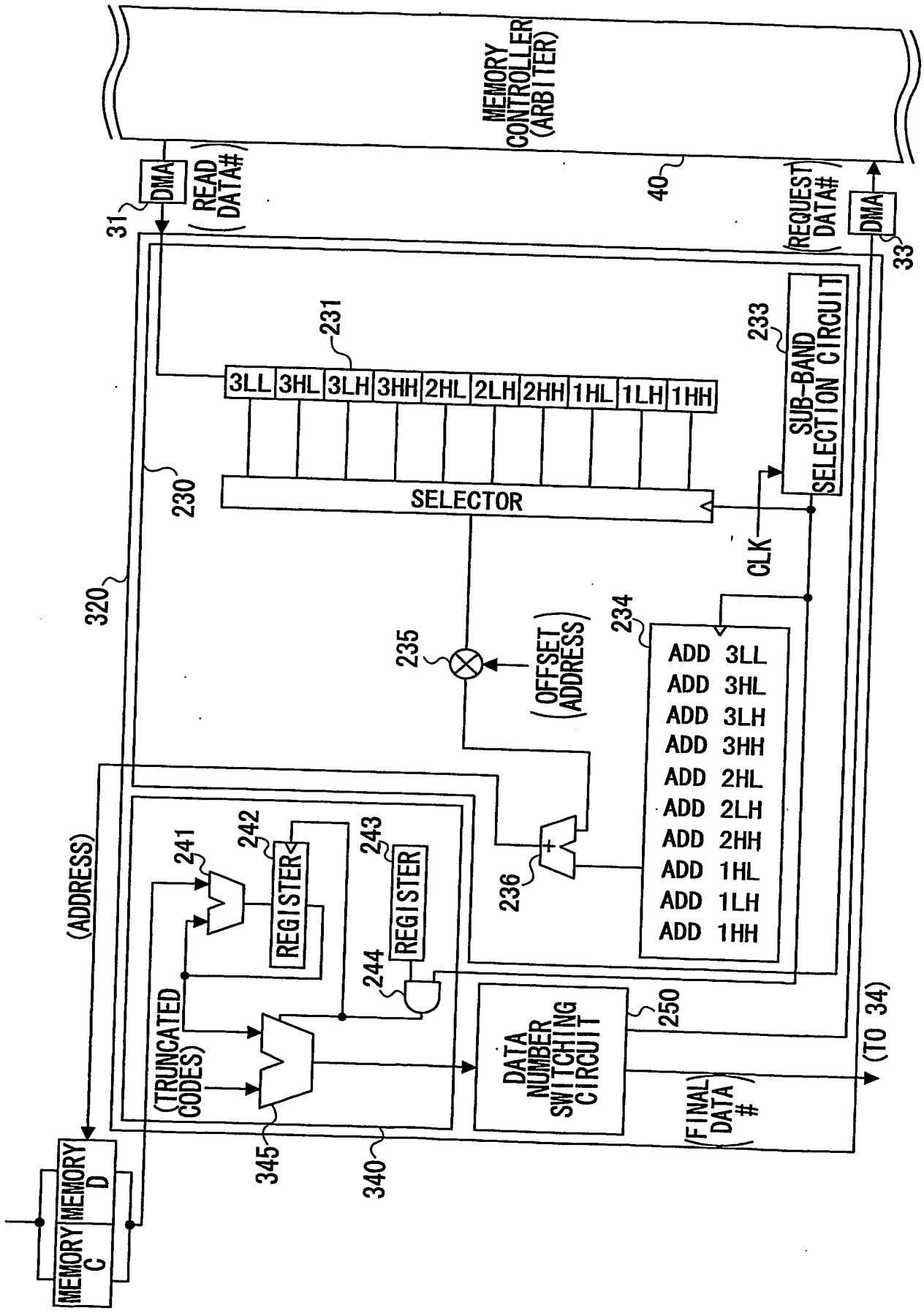

START
SB=1
S90
BP=0, SBP=0
S91
CB=1
S92
Q=BP+M(CB)
S93
CALCULATE SBP(CB)
S94
SBP=SBP+SBP(CB)
S95
CB=CB+1
S96
NO
CB>CBSB·MAX
S97
YES
WRITE SBP TO ADD"SB" + ADDOFF X BP
S98
BP=BP+1
S99
NO
BP>46
S100
YES
SB=SB+1
S101
NO
SB>10
S102
YES
END

FIG.19


MEMORY CONTROLLER (ARBITER)
40
DMA
31
READ DATA#
REQUEST DATA#
DMA
33
231
3LL 3HL 3LH 3HH 2HL 2LH 2HH 1HL 1LH 1HH
SELECTOR
230
233
SUB-BAND SELECTION CIRCUIT
CLK
320
235
(OFFSET ADDRESS)
234
ADD 3LL
ADD 3HL
ADD 3LH
ADD 3HH
ADD 2HL
ADD 2LH
ADD 2HH
ADD 1HL
ADD 1LH
ADD 1HH
236
241
242
REGISTER
243
REGISTER
244
(ADDRESS)
(TRUNCATED CODES)
345
340
DATA NUMBER SWITCHING CIRCUIT
250
(TO 34)
(FINAL DATA #)
MEMORY C
MEMORY D